miniCTR2 Project

May 2009

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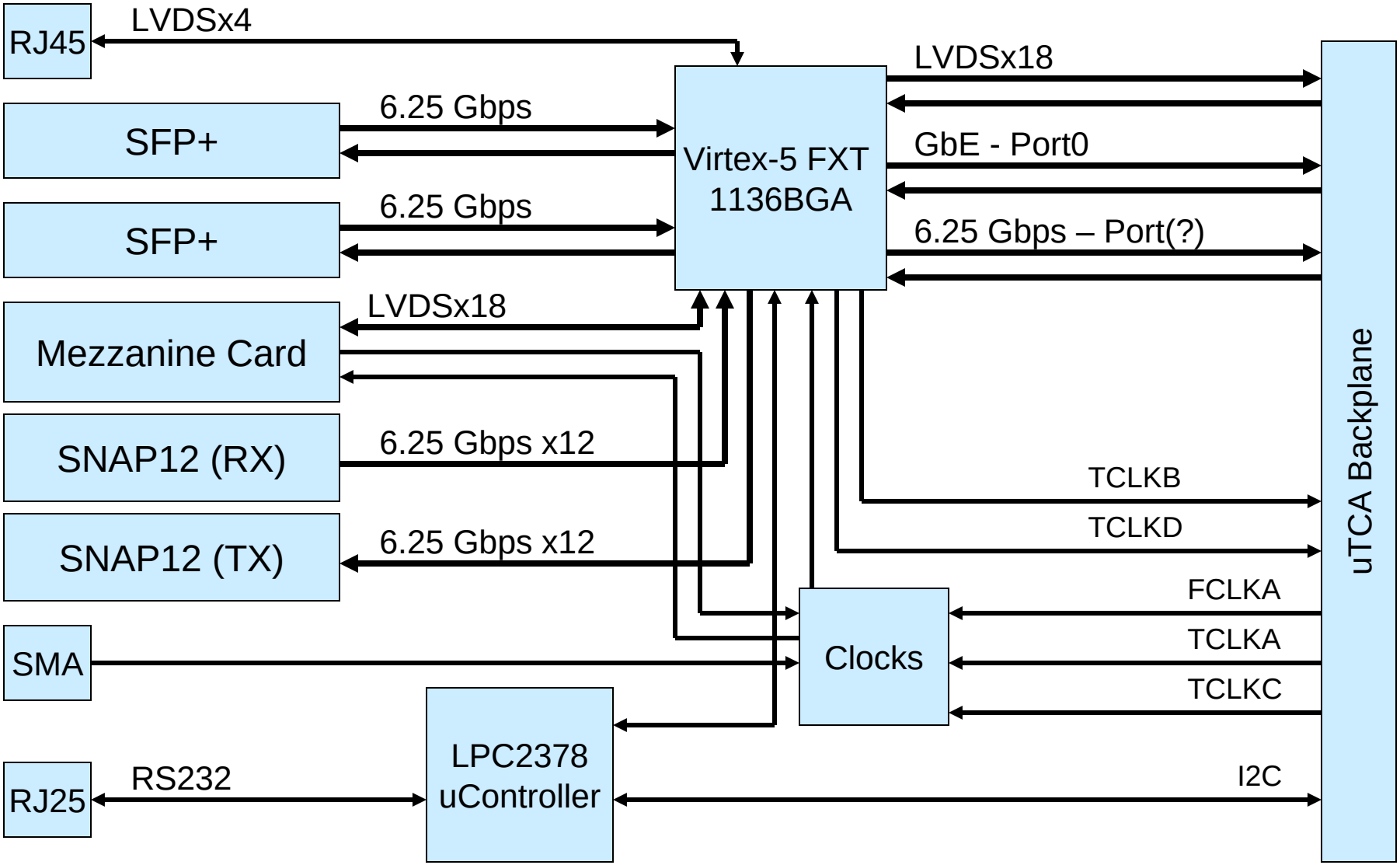
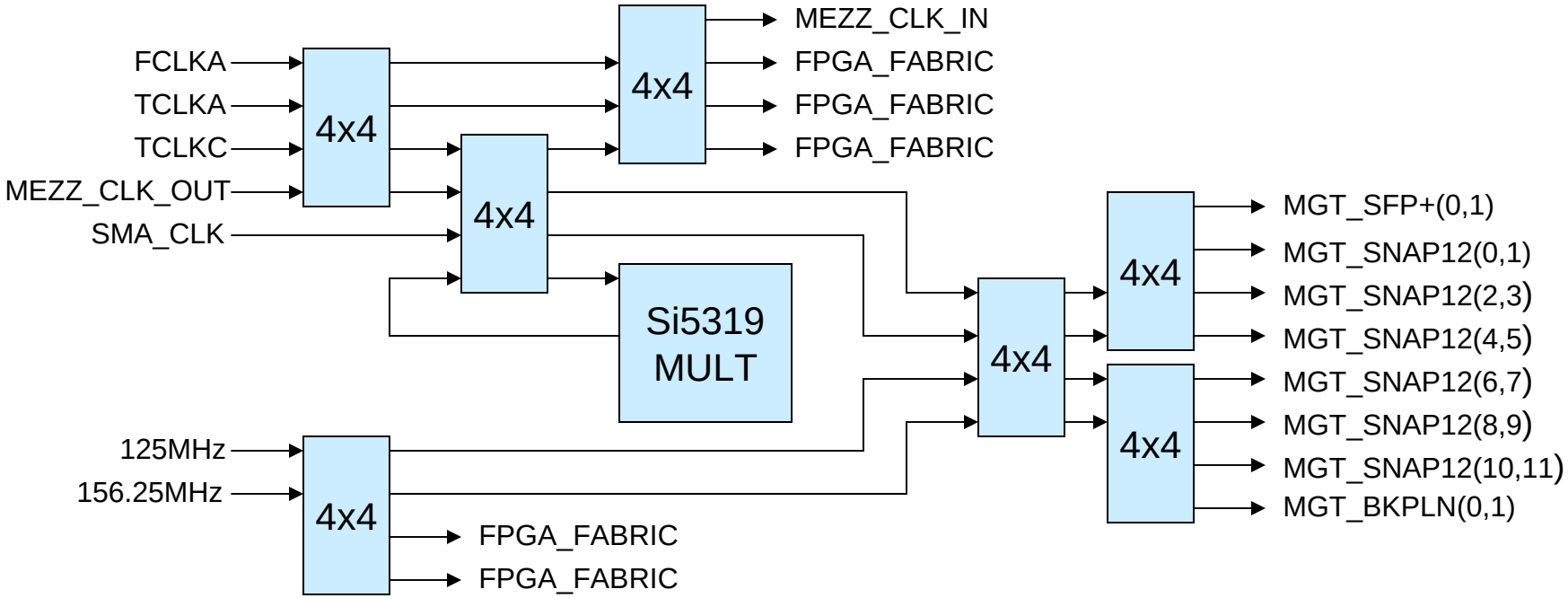
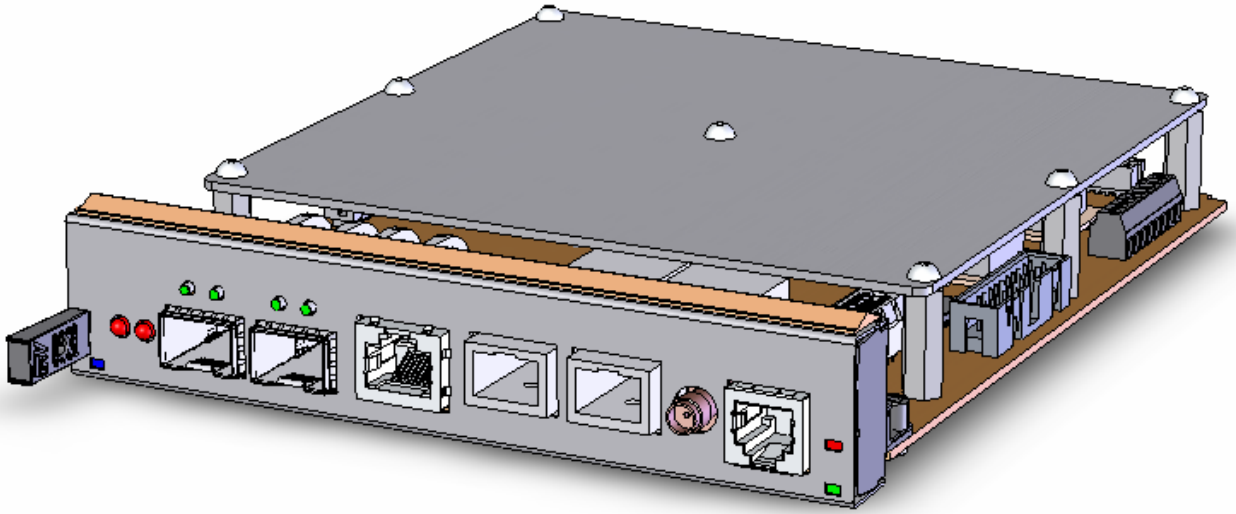


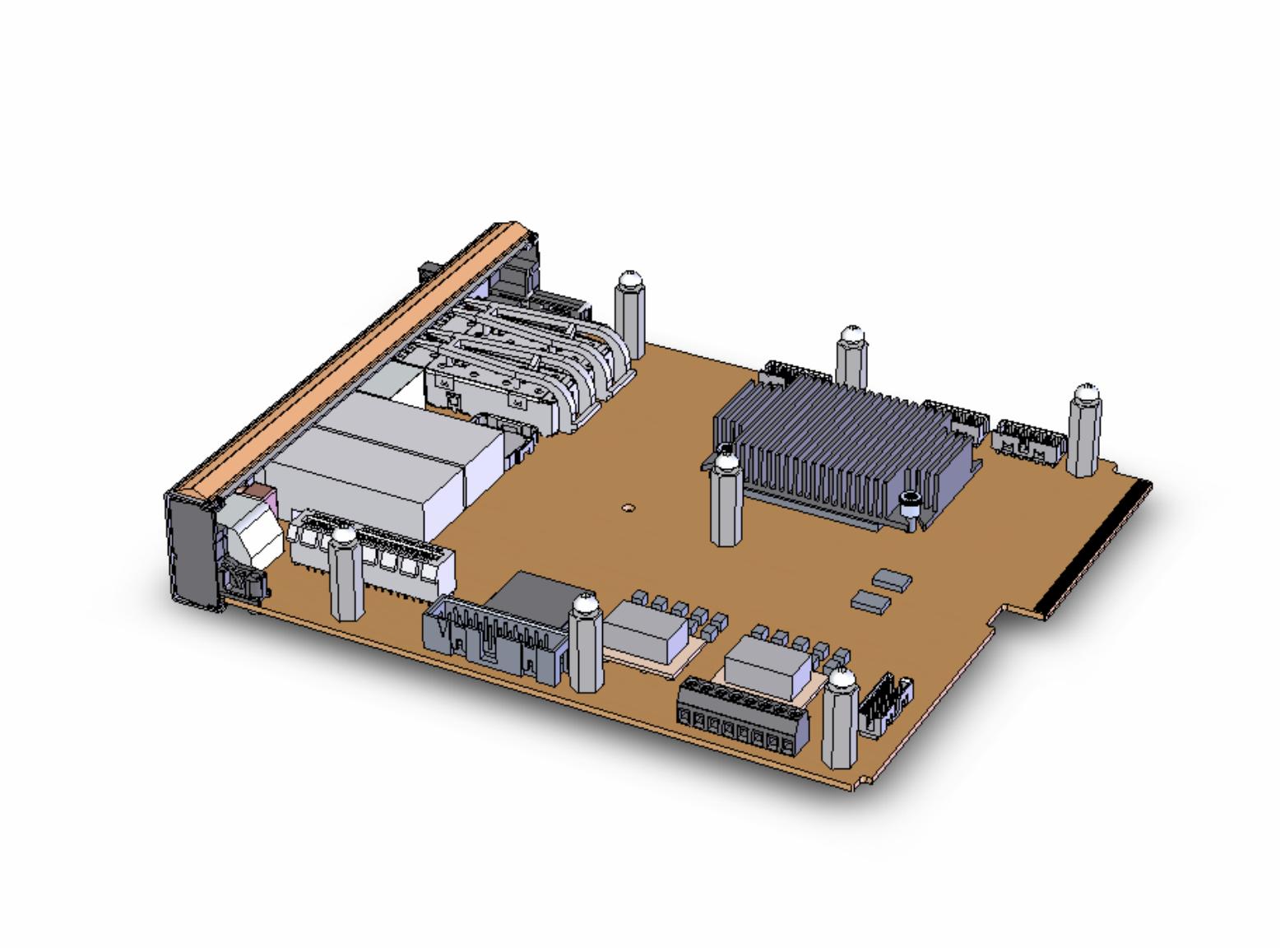
Block Diagram



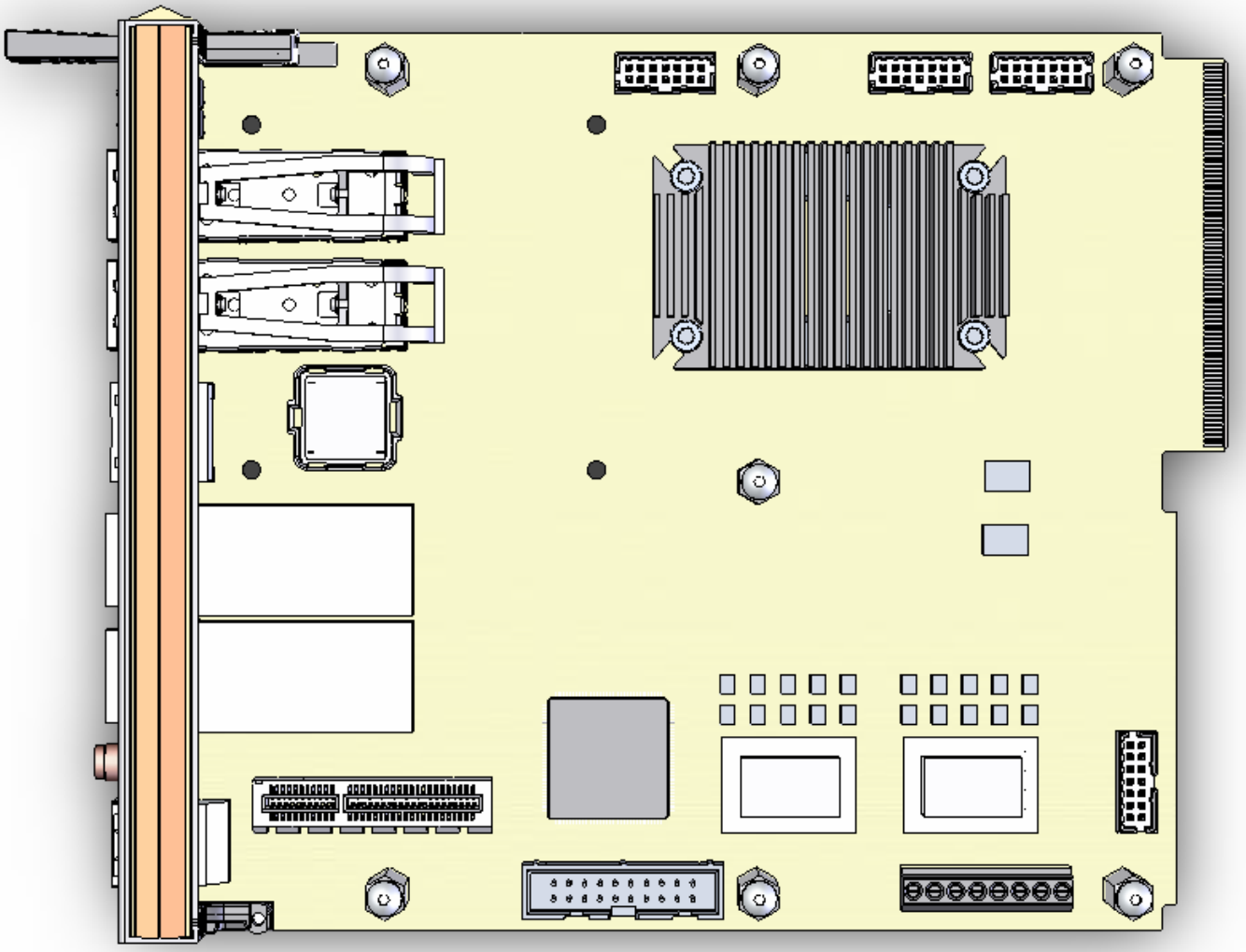
Clock Block Diagram



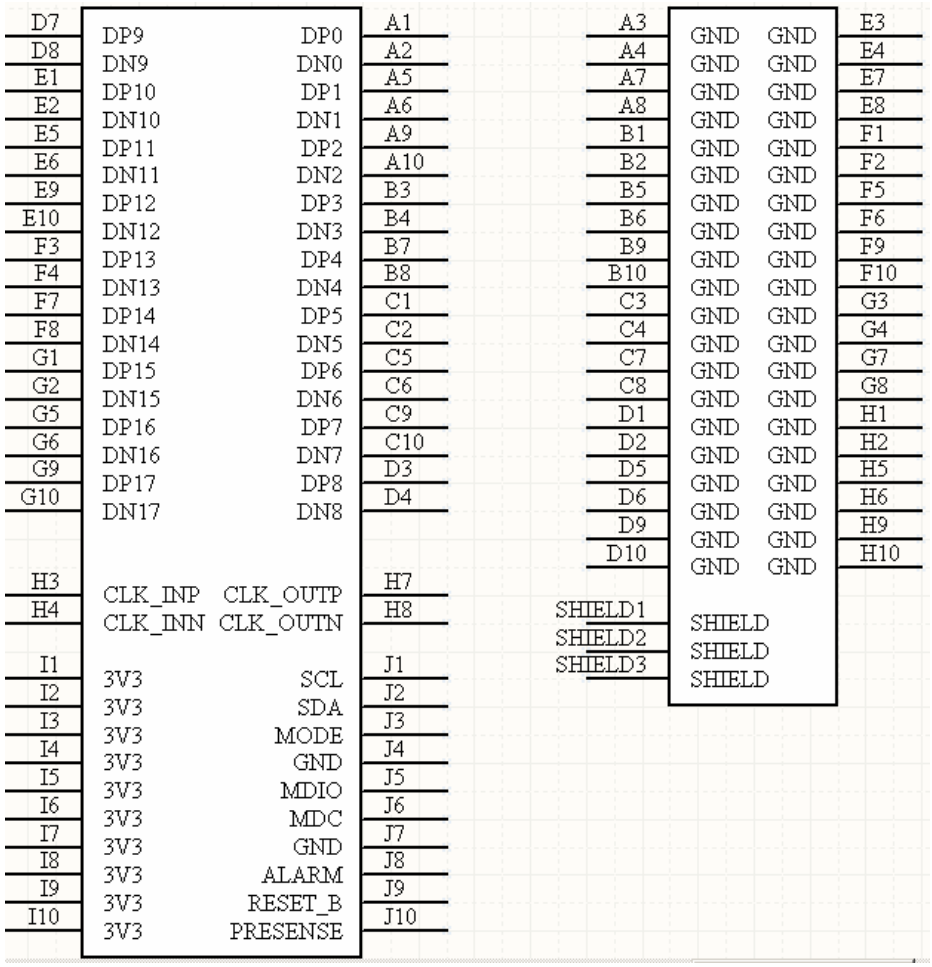
Front View

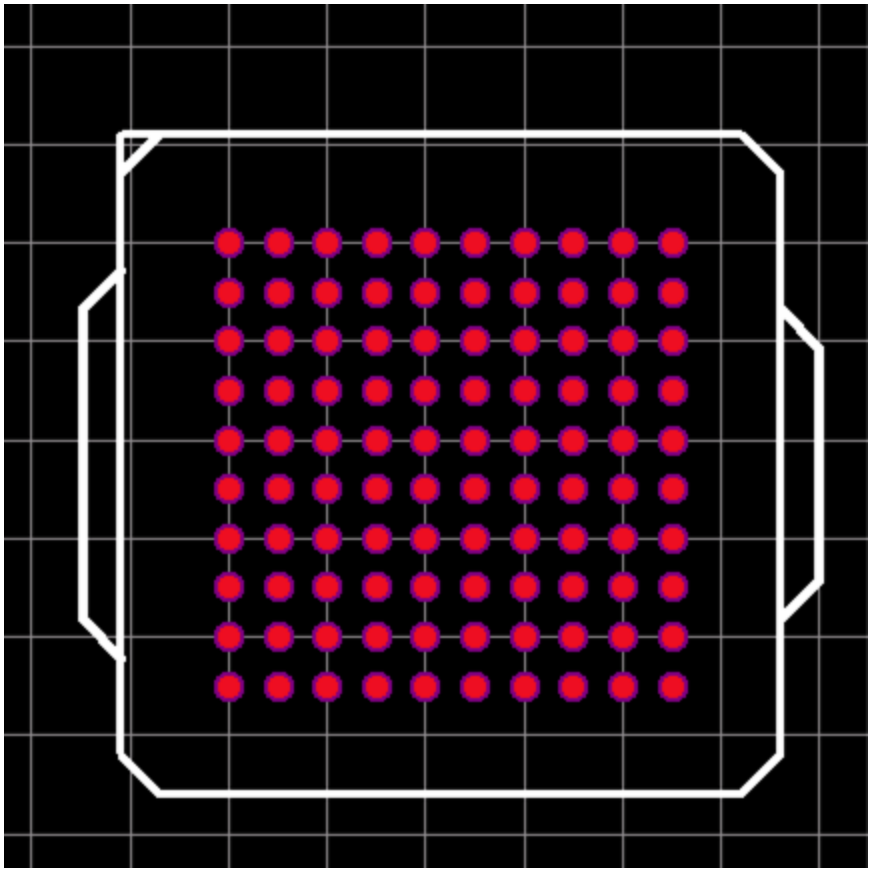


Rear View (without cover)



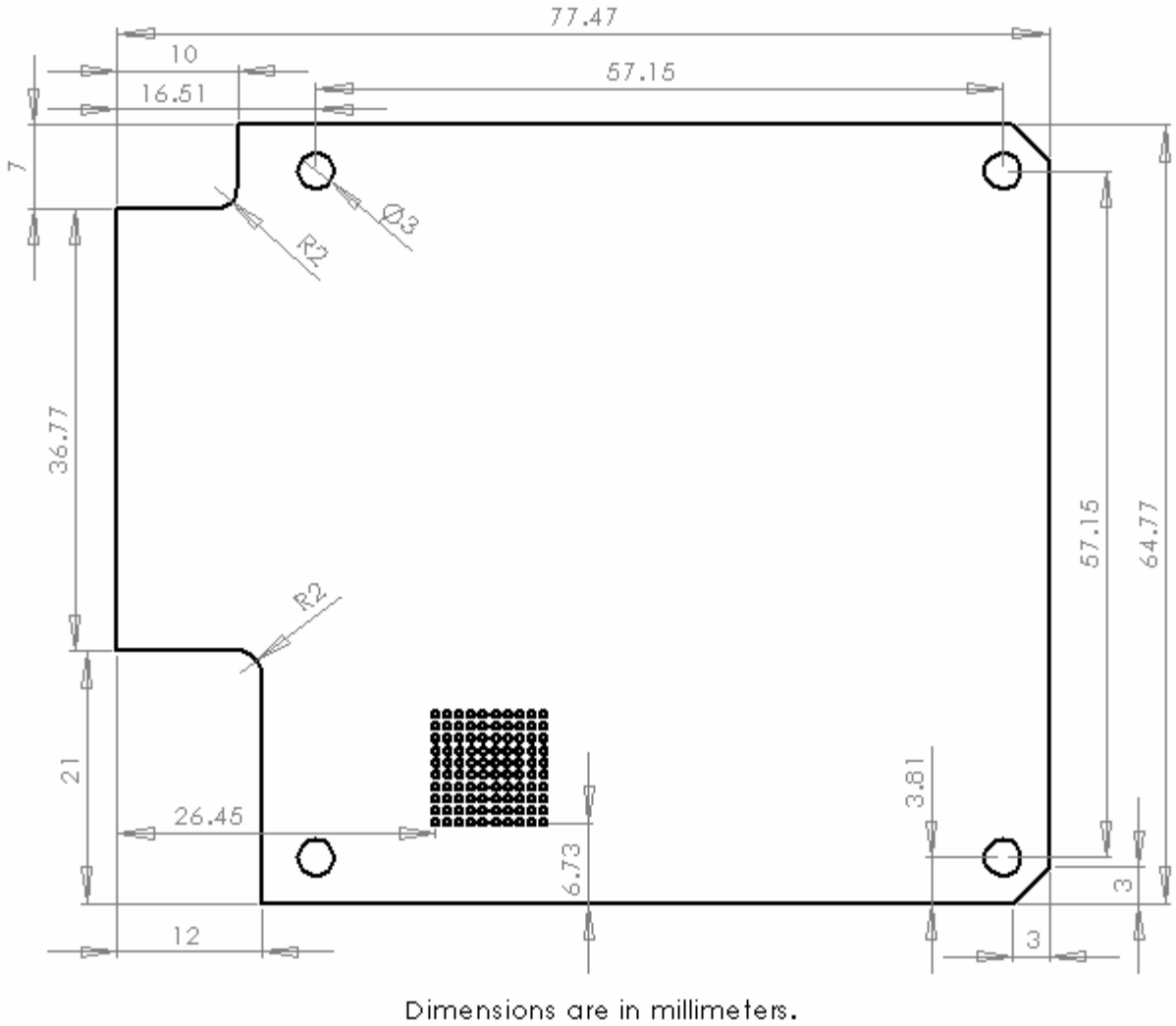
Top View (without cover)



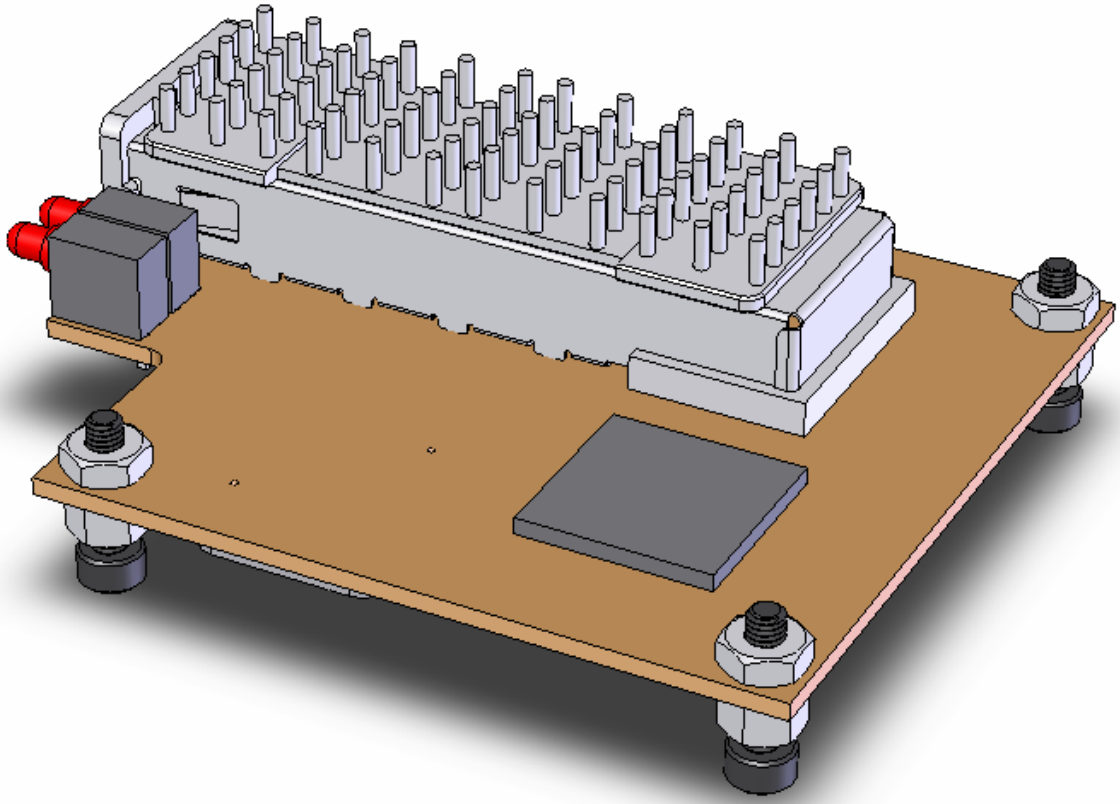


Mezzanine Connector: FCI 84512
miniCTR2 Connector: FCI 84513

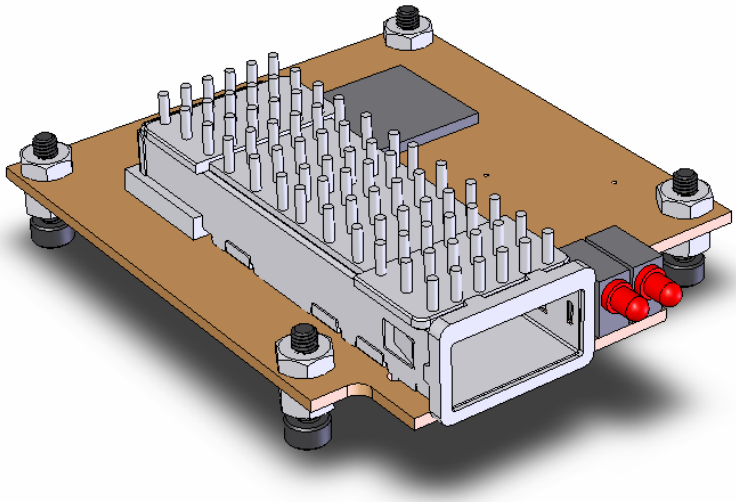
Mezzanine Card Interface

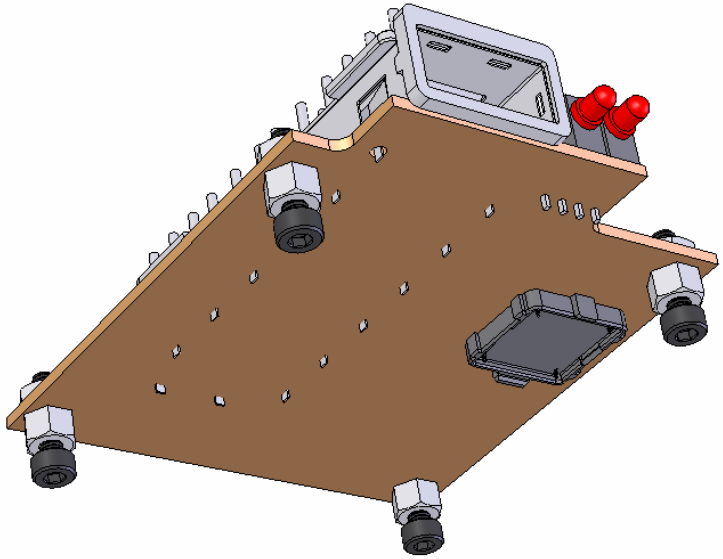


Mezzanine Card Dimensions

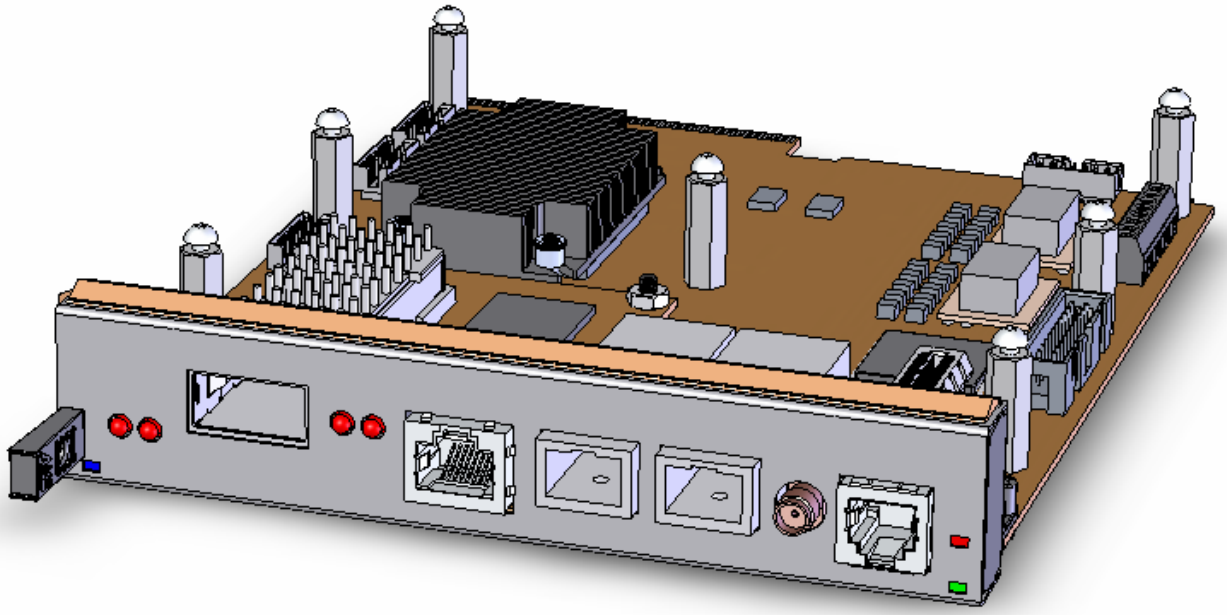


Mezzanine Card – with SERDES and XFP Module

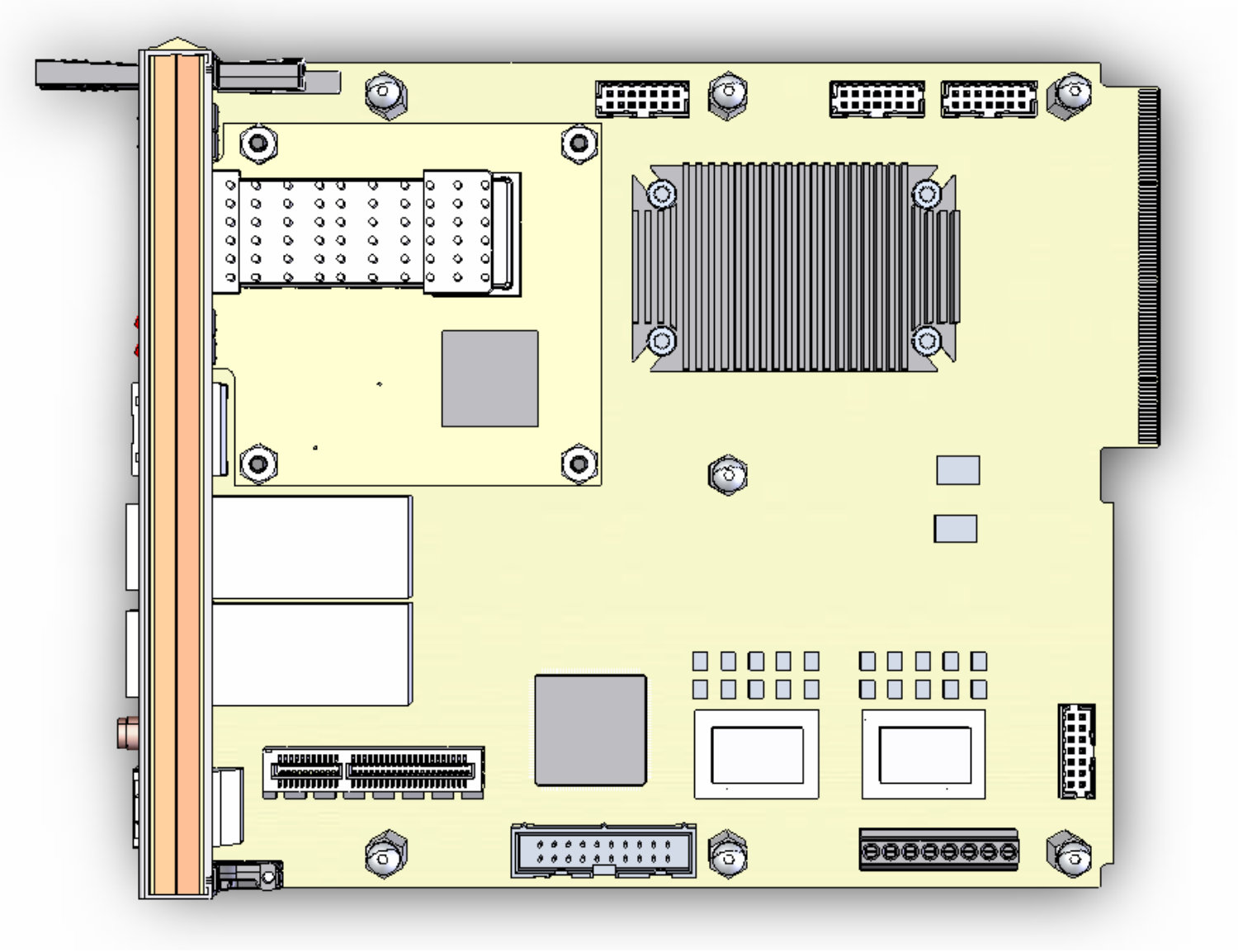




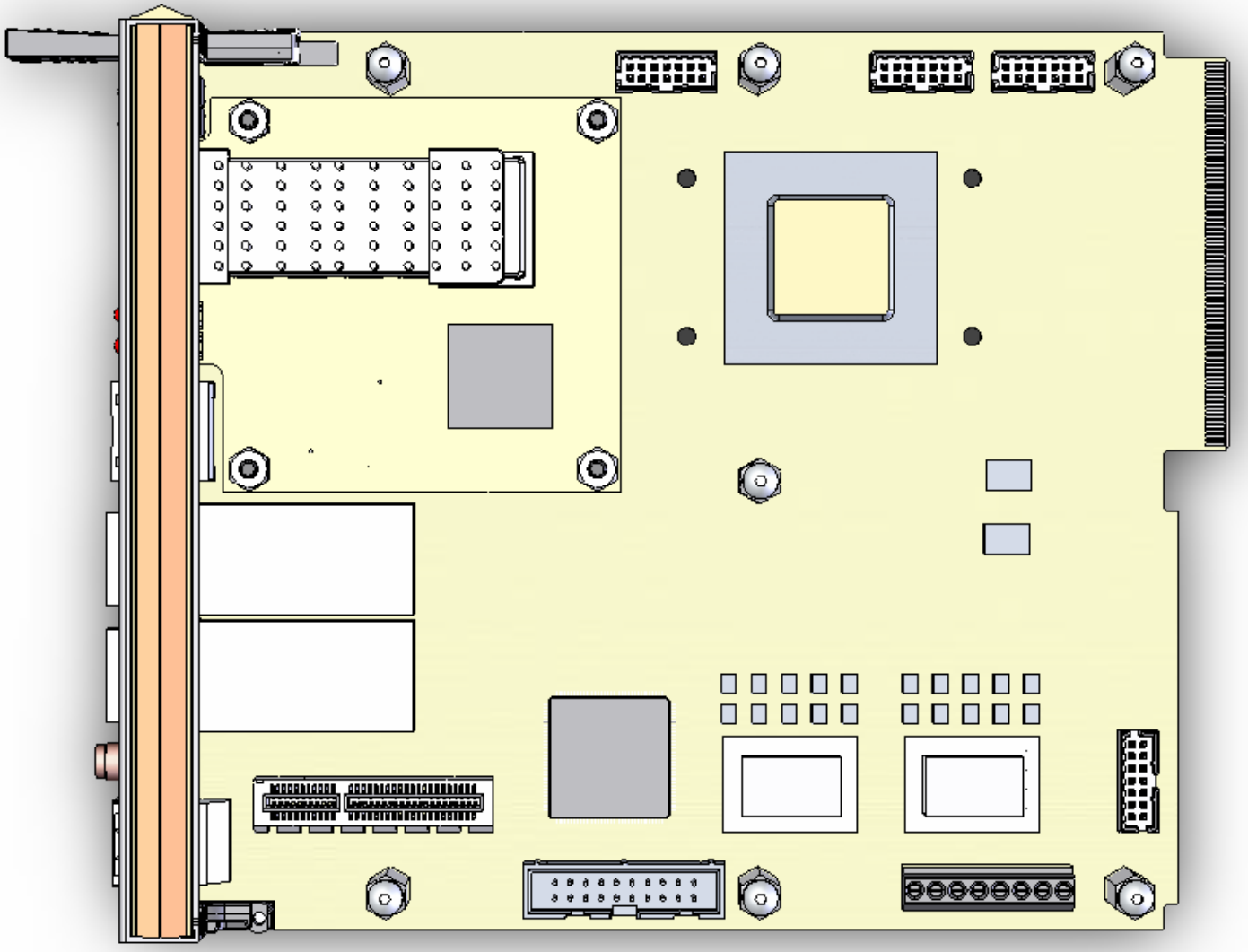
Mezzanine Card – with SERDES and XFP Module



Front View with Mezzanine Card



Top View with Mezzanine Card



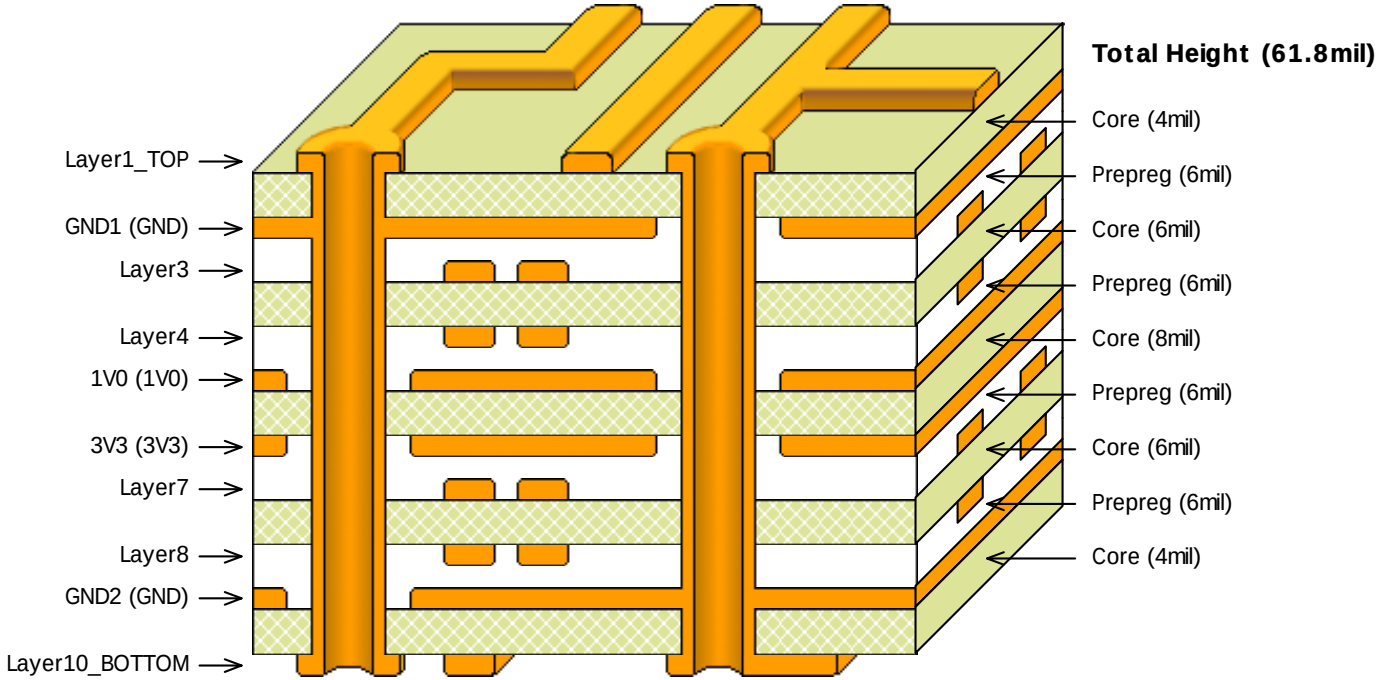
Top View with Mezzanine Card (no heatsink)

miniCTR1 bug fixes:

1) PowerEnable was pulled up to 3.3V power supply instead of 3.3V MANAGEMENT power supply. - fixed
2) Resistors for 3.3V and 1.0V power supplies were switched. - fixed
3) Linear power supply pullup for enable was incorrect. - fixed
4) Pullup for SFP LED was missing. - fixed
5) PORT0 P and N traces from FPGA were switched. - fixed
6) ESD strip was not configured for compliance with uTCA standard. - fixed
7) FPGA SM (System Monitor) was not disabled. - fixed
8) FPGA analog supply rails were not independently adjustable. - fixed
9) Microcontroller ISP (in-system-programming) capability was incorrect. - fixed
10) Microcontroller crystal was not identical to reference design. - fixed
11) Microcontroller LEDs were not identical to reference design. - fixed

Modifications for migration from LXT to FXT family of FPGAs:

1) MGTAVCCPLL is set to 1.0V (instead of 1.2V).
2) MGTRREF is 59ohms (instead of 50ohms).



PCB Layer Stackup

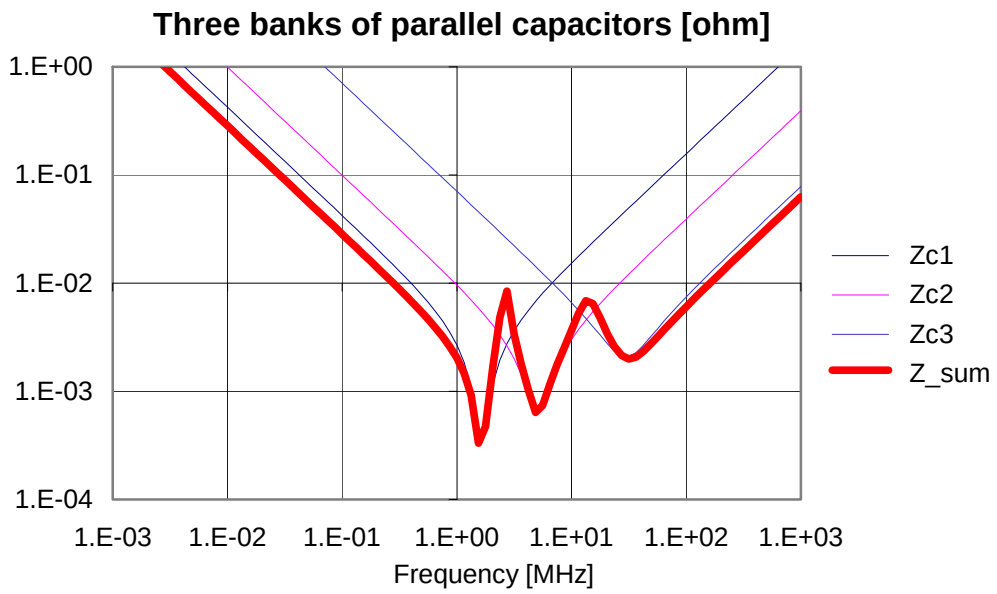
Layer Name	FR-4 (mils)	copper (mils)	line (mils)	space (mils)	SE (ohms)	Diff (ohms)
Layer1_TOP		0.7	6	12	51	100
	4					
GND1		1.4				
	6					
Layer3		0.7	5	15	53	102
	6					
Layer4		0.7	5	15	53	102
	6					
1V0		1.4				
	8					
3V3		1.4				
	6					
Layer7		0.7	5	15	53	102
	6					
Layer8		0.7	5	15	53	102
	6					
GND2		1.4				
	4					
Layer10_BOTTOM		0.7	6	12	51	100
	52	9.8				

See: www.icd.com.au/Diff_Calc/10_layer_stackup.htm
(Assume FR-4 has dielectric constant of 4.7)

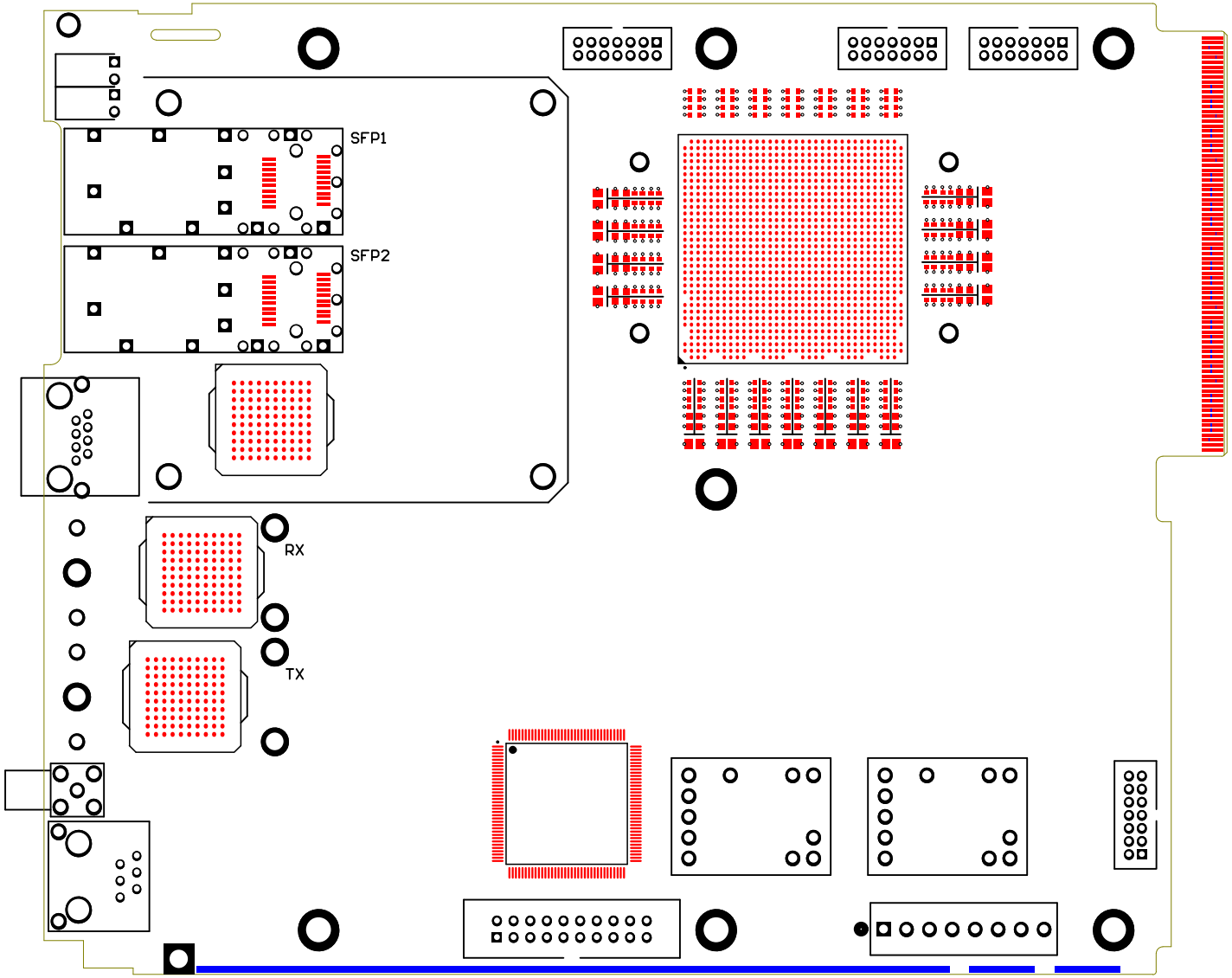
PCB Transmission Line Impedance

Parallel impedance of three groups of FPGA 1.0V core power supply capacitors

Three values of parallel bypass caps	C1	C2	C3	
Capacitance C [microF]:	4.7	1	0.047	Fmin[Hz]
				1.00E+03
Ser. resistance ESR [ohms]:	0.001	0.01	0.1	Fmax[Hz]
				1.00E+09
Ser. inductance ESL [nH]:	2	1	0.6	
				Total:
Number of caps in each value:	8	16	48	72



1.0V FPGA Core Power Supply Impedance



miniCTR2 Placement of Critical Components